REMARKS

Claims remaining in the present patent application are Claims 1-20.

35 USC § 102

Claims 1-6, 8-15 and 17-20 stand rejected under 35 USC § 102(e) as being

allegedly anticipated by Pearce et al. (US 5,973,368; "Pearce"). Applicants have

reviewed the cited reference and respectfully assert that embodiments of the present

invention as recited in Claims 1-6, 8-15 and 17-20 are not anticipated or rendered

obvious by Pearce.

Applicants understand Pearce to describe a monolithic class D amplifier. As

used in Pearce and the semiconductor arts, the term "monolithic" means

"constituting or acting as a single, often rigid, uniform whole." Thus, Pearce describes

an integrated circuit that has no function beyond amplification. Consequently,

Pearce does not teach, suggest or disclose embodiments in accordance the present

that recite limitations beyond those of an amplifier, for example, limitations drawn to

a microcontroller chip comprising a processor for executing program instructions, as

recited by Claims 1-20. For this reason, Applicants respectfully assert that Claims

1-20 overcome the rejections of record and respectfully solicit allowance of these

Claims.

Regarding Claim 1, Applicants respectfully assert that Pearce does not teach,

suggest or disclose the limitation of "a processor for executing program instructions"

as recited in independent Claim 1. The rejection alleges that "control logic" of column

CYPR-CD00231/ACM/NAO Examiner: Woo, S. L.

Serial No. 09/893,048 Group Art Unit: 2643

-2-

6 lines 20-22 comprise the recited processor. Applicants respectfully traverse. The

referenced control logic is described vaguely in Pearce as merely for monitoring power

in a QVDMOS power device (column 6, lines 22-24). However, Pearce is silent as to

any suggestion that such "control logic" comprises a processor or executes program

instructions. For this reason, Applicants respectfully assert that Claim 1 overcomes

the rejections of record and respectfully solicit allowance of this Claim.

Further with regard to Claim 1, Applicants respectfully assert that Pearce

does not teach, suggest or disclose the limitation of "an array of configurable circuit

blocks" as recited in independent Claim 1. The rejection alleges that array 3.10 of

Pearce comprises such a configurable array. Applicants respectfully traverse. There

is nothing in Pearce to suggest that array 3.10, or anything else, within Pearce is

configurable as claimed. For this additional reason, Applicants respectfully assert

that Claim 1 overcomes the rejections of record and respectfully solicit allowance of

this Claim.

Further still with regard to the embodiment of Claim 1, Applicants respectfully

assert that Pearce does not teach, suggest or disclose the limitation of "an analog

amplifier" "on a microcontroller chip" as recited in independent Claim 1. Applicants

understand Pearce to describe "a monolithic integrated circuit... to drive the voicecoil

of the speaker." (Abstract) As described previously, Pearce is silent as to any

suggestion that the monolithic integrated circuit comprises a processor or executes

program instructions as claimed. Further, Pearce is silent as to any suggestion that

the monolithic integrated circuit performs any function commonly associated with a

microcontroller. For this yet additional reason, Applicants respectfully assert that

CYPR-CD00231/ACM/NAO Examiner: Woo, S. L.

Serial No. 09/893,048 Group Art Unit: 2643

-3-

Claim 1 overcomes the rejections of record and respectfully solicit allowance of this

Claim.

Claims 2-10 depend from Claim 1. Applicants respectfully solicit allowance of

these Claims as they depend from an allowable base claim.

Further with regard to Claim 2, Applicants respectfully assert that Pearce

does not teach, suggest or disclose the limitation of "wherein the on-chip analog

amplifier is situated adjacent one of the four corners" as recited in Claim 2.

Applicants respectfully note that the rejection does not address this limitation and

respectfully assert that Pearce is silent as to any preferential positioning of an

amplifier relative to a corner of an integrated circuit. For this additional reason,

Applicants respectfully assert that Claim 2 overcomes the rejections of record and

respectfully solicit allowance of this Claim.

Further with regard to Claim 4, Applicants respectfully assert that Pearce

does not teach, suggest or disclose the limitation of "a tristateable CMOS analog

amplifier" as recited in Claim 4. Applicants respectfully note that the rejection does

not address this limitation and respectfully assert that Pearce is silent as to

tristateable analog circuitry. For this additional reason, Applicants respectfully

assert that Claim 4 overcomes the rejections of record and respectfully solicit

allowance of this Claim.

With regard to Claim 11, Applicants respectfully assert that Pearce does not

teach, suggest or disclose the limitation of "a processor for executing program

CYPR-CD00231/ACM/NAO Examiner: Woo, S. L. Serial No. 09/893,048 Group Art Unit: 2643

-4-

instructions" as recited in independent Claim 11, for the rationale presented

previously with respect to Claim 1. For this reason, Applicants respectfully assert

that Claim 11 overcomes the rejections of record and respectfully solicit allowance of

this Claim.

Further with regard to Claim 11, Applicants respectfully assert that Pearce

does not teach, suggest or disclose the limitation of "an array of configurable digital

circuit blocks" as recited in independent Claim 11. Applicants respectfully note that

the rejection does not address this limitation and respectfully assert that Pearce is

silent as to any configurable digital circuitry. For this additional reason, Applicants

respectfully assert that Claim 11 overcomes the rejections of record and respectfully

solicit allowance of this Claim.

Further still with regard to Claim 11, Applicants respectfully assert that

Pearce does not teach, suggest or disclose the limitation of "an array of configurable

digital circuit blocks configured to perform a digital circuit function" as recited in

independent Claim 11. Applicants respectfully note that the rejection does not

address this limitation and respectfully assert that Pearce is silent as to any

configurable digital circuitry, much less as to digital circuit blocks configured to

perform a digital circuit function. For this still additional reason, Applicants

respectfully assert that Claim 11 overcomes the rejections of record and respectfully

solicit allowance of this Claim.

Further yet with regard to Claim 11, Applicants respectfully assert that

Pearce does not teach, suggest or disclose the limitation of "an array of configurable

CYPR-CD00231/ACM/NAO

Serial No. 09/893,048 Group Art Unit: 2643

Examiner: Woo, S. L.

analog circuit blocks" as recited in independent Claim 11. Applicants respectfully

note that the rejection does not address this limitation and respectfully assert that

Pearce is silent as to any configurable analog circuitry. For this yet additional reason,

Applicants respectfully assert that Claim 11 overcomes the rejections of record and

respectfully solicit allowance of this Claim.

Still further yet with regard to Claim 11, Applicants respectfully assert that

Pearce does not teach, suggest or disclose the limitation of "an on-chip CMOS analog

amplifier" as recited by Claim 11. On the contrary, Pearce teaches a QVDMOS class

D amplifier. As is well known in the art, a class D amplifier is not an analog amplifier.

as a class D amplifier utilizes quantized signals. Further, as is well known in the art,

QVDMOS is not CMOS. For these still yet additional reasons, Applicants

respectfully assert that Claim 11 overcomes the rejections of record and respectfully

solicit allowance of this Claim.

Claims 12-17 depend from Claim 11. Applicants respectfully solicit allowance

of these Claims as they depend from an allowable base claim.

Further with regard to Claim 12, Applicants respectfully assert that Pearce

does not teach, suggest or disclose the limitation of "wherein the on-chip analog

amplifier is situated adjacent one of the four corners (of the chip)" as recited in Claim

12. Applicants respectfully note that the rejection does not address this limitation

and respectfully assert that Pearce is silent as to any preferential positioning of an

amplifier relative to a corner of an integrated circuit. For this additional reason,

CYPR-CD00231/ACM/NAO Examiner: Woo, S. L.

Serial No. 09/893,048

-6-

Applicants respectfully assert that Claim 12 overcomes the rejections of record and

respectfully solicit allowance of this Claim.

Further with regard to Claim 15, Applicants respectfully assert that Pearce

does not teach, suggest or disclose the limitation of "a tristatable CMOS analog

amplifier" as recited in Claim 15. Applicants respectfully note that the rejection does

not address this limitation and respectfully assert that Pearce is silent as to

tristateable analog circuitry. For this additional reason, Applicants respectfully

assert that Claim 15 overcomes the rejections of record and respectfully solicit

allowance of this Claim.

With respect to Claim 18, Applicants respectfully assert that Pearce does not

teach, suggest or disclose the limitation of "a processor for executing program

instructions" as recited in independent Claim 11, for the rationale presented

previously with respect to Claim 1. For this reason, Applicants respectfully assert

that Claim 18 overcomes the rejections of record and respectfully solicit allowance of

this Claim.

Further with regard to Claim 18, Applicants respectfully assert that Pearce

does not teach, suggest or disclose the limitation of "an array of configurable digital

circuit blocks" as recited in independent Claim 18, for the rationale presented

previously with respect to Claim 11. For this additional reason, Applicants

respectfully assert that Claim 18 overcomes the rejections of record and respectfully

solicit allowance of this Claim.

CYPR-CD00231/ACM/NAO Examiner: Woo, S. L. Serial No. 09/893,048 Group Art Unit: 2643

-7-

Further still with regard to Claim 18, Applicants respectfully assert that

Pearce does not teach, suggest or disclose the limitation of "an array of configurable

digital circuit blocks configured to perform a digital circuit function" as recited in

independent Claim 18, for the rationale presented previously with respect to Claim

11. For this still additional reason, Applicants respectfully assert that Claim 18

overcomes the rejections of record and respectfully solicit allowance of this Claim.

Further yet with regard to Claim 18, Applicants respectfully assert that

Pearce does not teach, suggest or disclose the limitation of "an array of configurable

analog circuit blocks" as recited in independent Claim 18, for the rationale presented

previously with respect to Claim 11. For this yet additional reason, Applicants

respectfully assert that Claim 18 overcomes the rejections of record and respectfully

solicit allowance of this Claim.

Still further yet with regard to Claim 18, Applicants respectfully assert that

Pearce does not teach, suggest or disclose the limitation of "an on-chip tristateable

CMOS analog amplifier" as recited by Claim 18, for the rationale presented

previously with respect to Claim 11. Further, Pearce is silent as to tristateable

analog circuitry. For these still yet additional reasons, Applicants respectfully assert

that Claim 18 overcomes the rejections of record and respectfully solicit allowance of

this Claim.

Still with reference to Claim 18, Applicants respectfully assert that Pearce

does not teach, suggest or disclose the limitation of "a switchable current source for

selectively providing an increase in bias current... under control of the processor" as

CYPR-CD00231/ACM/NAO

Serial No. 09/893,048 Group Art Unit: 2643

-8-

recited by Claim 18. Applicants reiterate that Pearce does not teach, suggest or

disclose a processor, for the rationale presented with respect to Claim 1.

Further, the rejection refers to shutting off the QVDMOS bridge if the current

exceeds predetermine(d) limits. Applicants respectfully assert that one of ordinary

skill in the art would understand a vast difference between turning off an amplifier as

taught by Pearce and increasing bias current as recited by the instant claim.

According to Pearce, the amplifier ceases function. In contrast, in accordance with

embodiments of the present invention, an amplifier continues to amplify. For these

additional reasons, Applicants respectfully assert that Claim 18 overcomes the

rejections of record and respectfully solicit allowance of this Claim.

Once more with respect to Claim 18, Applicants respectfully assert that

Pearce does not teach, suggest or disclose the limitation of "on-chip analog amplifier is

situated adjacent one of the four corners" as recited by Claim 18. Applicants

reiterate that Pearce does not teach, suggest or disclose an analog amplifier, for the

rationale previously presented with respect to Claim 11.

Further, Applicants respectfully assert that Pearce is silent as to any

preferential positioning of an amplifier relative to a corner of an integrated circuit, and

respectfully note that the rejection does not address this limitation. For these

additional reasons, Applicants respectfully assert that Claim 18 overcomes the

rejections of record and respectfully solicit allowance of this Claim.

CYPR-CD00231/ACM/NAO Examiner: Woo, S. L.

Serial No. 09/893,048 Group Art Unit: 2643

Claims 19-20 depend from Claim 18. Applicants respectfully solicit allowance of these Claims as they depend from an allowable base claim.

## **CONCLUSION**

Claims remaining in the present patent application are Claims 1-20.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Applicants have reviewed the following reference that was cited but not relied upon and do not find this reference to teach or suggest the present claimed invention: US 6,079,985.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO LLP

Anthony C. Murabito

Reg. No. 35,295

Two North Market Street Third Floor San Jose, California 95113 (408) 938-9060